What is Claimed is:

1. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of pairs of first and second conductive patterns are formed, each pair of the first and second conductive patterns being spaced apart from each other and formed at both ends of the first sheet, each pair of the first and second conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a third conductive pattern is formed, the third conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of resistive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, at least one end of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

2. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of pairs of first and second conductive patterns are formed, each pair of the first and second conductive patterns being spaced apart from each other and formed at both ends of the first sheet, each pair of the first and second conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a third conductive pattern is formed, the third conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of inductive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, at least one end of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

3. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of pairs of first and second conductive patterns are formed, each pair of the first and second conductive patterns being spaced apart from each other and formed at both ends of the first sheet, each pair of the first and second conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a third conductive pattern is formed, the third conductive pattern consisting of first and second portions which are spaced apart from each other and formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of resistive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, both opposite ends of the first and second portions of the third conductive pattern are connected to third and fourth external terminals, which are common terminals, respectively, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

4. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of pairs of first and second conductive patterns are formed, each pair of the first and second conductive patterns being spaced

apart from each other and formed at both ends of the first sheet, each pair of the first and second conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a third conductive pattern is formed, the third conductive pattern consisting of first and second portions which are spaced apart from each other and formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of inductive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, both opposite ends of the first and second portions of the third conductive pattern are connected to third and fourth external terminals, which are common terminals, respectively, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

5. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of resistive patterns formed corresponding to the unit elements on the first to third sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals,

respectively, at least one end of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first to third sheets are laminated so that at least one of the third sheet is interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

6. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of inductive patterns formed corresponding to the unit elements on the first to third sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, at least one end of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively, the first to third sheets are laminated so that at least one of the third sheet is interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

7. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed

in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet;

at least one fourth sheet on which a fourth conductive pattern is formed, the fourth conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of resistive patterns formed corresponding to the unit elements on the first to fourth sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, both opposite ends of the third and fourth conductive patterns are connected to third and fourth external terminals, which are common terminals, respectively, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first to fourth sheets are laminated so that the third and fourth sheets are interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

8. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third

conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet;

at least one fourth sheet on which a fourth conductive pattern is formed, the fourth conductive pattern being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of inductive patterns formed corresponding to the unit elements on the first to fourth sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, both opposite ends of the third and fourth conductive patterns are connected to third and fourth external terminals, which are common terminals, respectively, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively, the first to fourth sheets are laminated so that the third and fourth sheets are interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

9. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third conductive pattern comprising a plurality of first portions formed in the same direction as the first conductive patterns and a second portion connected to one ends of the first portions, each of the first portions being arranged in each of the unit elements, the second portion being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of resistive patterns formed corresponding to the unit elements on the

first to third sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, at least one end of the second portion of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first to third sheets are laminated so that at least one of the third sheet is interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

10. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed in a direction of both ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements;

at least one third sheet on which a third conductive pattern is formed, the third conductive pattern comprising a plurality of first portions formed in the same direction as the first conductive patterns and a second portion connected to one ends of the first portions, each of the first portions being arranged in each of the unit elements, the second portion being formed over the unit elements in a transverse direction of both the ends of the first sheet; and

a plurality of inductive patterns formed corresponding to the unit elements on the first to third sheets,

wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, which are input and output terminals, respectively, at least one end of the second portion of the third conductive pattern is connected to a third external terminal, which is a common terminal, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively,

the first to third sheets are laminated so that at least one of the third sheet is interposed between the first and second sheets, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

11. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed, each of the first conductive patterns consisting of first to third portions, the first and second portions being spaced apart from each other and formed at both ends of the first sheet, the third portion being spaced apart from the first and second portions and formed in a transverse direction of both the ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed, each of the second conductive patterns consisting of fourth and fifth portions spaced from each other, the fourth portion partially overlapping with the first and third portions, the fifth portion partially overlapping with the second and third portions, each of the second conductive patterns being arranged in each of the unit elements; and

a plurality of resistive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second portions are connected to first and second external terminals, which are input and output terminals, respectively, the third portions are connected to each other over the unit elements, at least one end of the connected third portions is connected to a third external terminal, which is a common terminal, both ends of each of the resistive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

12. A laminated chip element comprising a plurality of unit elements, comprising:

at least one first sheet on which a plurality of first conductive patterns are formed, each of the first conductive patterns consisting of first to third portions, the first and second portions being spaced apart from each other and formed at both ends of the first sheet, the

third portion being spaced apart from the first and second portions and formed in a transverse direction of both the ends of the first sheet, each of the first conductive patterns being arranged in each of the unit elements;

at least one second sheet on which a plurality of second conductive patterns are formed, each of the second conductive patterns consisting of fourth and fifth portions spaced from each other, the fourth portion partially overlapping with the first and third portions, the fifth portion partially overlapping with the second and third portions, each of the second conductive patterns being arranged in each of the unit elements; and

a plurality of inductive patterns formed corresponding to the unit elements on the first and second sheets,

wherein one ends of the first and second portions are connected to first and second external terminals, which are input and output terminals, respectively, the third portions are connected to each other over the unit elements, at least one end of the connected third portions is connected to a third external terminal, which is a common terminal, both ends of each of the inductive patterns are connected to the first and second external terminals, respectively, the first and second sheets are alternately laminated, and a protective insulation layer is formed on the uppermost one of the laminated sheets.

13. The laminated chip element according to any one of claims 1 to 12, wherein areas of overlapping portions between the conductive patterns differ from each other.

14. The laminated chip element according to any one of claims 1, 3, 5, 7, 9 and 11, wherein pairs of metal pads are formed to be spaced each other, and each of the resistive patterns is formed so that the resistive pattern connects a pair of the metal pads to each other.

15. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein pairs of metal pads are formed to be spaced each other, and each of the inductive patterns is formed so that the inductive pattern connects a pair of the metal pads to each other.

16. The laminated chip element according to any one of claims 1 to 12, wherein the protective insulation layer includes epoxy or glass.

17. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein some of the inductive patterns of the unit elements are formed on an upper surface of the laminated chip element, and the other of the inductive patterns of the unit elements are formed on a lower surface of the laminated chip element.

18. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein the inductive pattern is spiral, an insulated bridge is formed in a radial direction across the spiral inductive pattern, and a bridge pattern for extending a central end of the inductive pattern to an outside thereof is formed on the insulated bridge.

19. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein a ferrite layer is form on the laminated chip element, and the inductive pattern is formed on the ferrite layer.

20. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein the inductive pattern includes resistive material, such as Ni-Cr, RuO_2.

21. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein a plurality of inductor sheets are further laminated, at least one of the inductive patterns are formed on each of the inductor sheets, and both ends of the respective inductive patterns are connected to the corresponding first and second external terminals.

22. The laminated chip element according to any one of claims 2, 4, 6, 8, 10 and 12, wherein a plurality of inductor sheets are further laminated, an inductive pattern is formed on each of the inductor sheets, the inductive patterns are connected to each other in series through through holes formed in the inductor sheets, both ends of the connected inductive

patterns are connected to the first and second external terminals, respectively.

23. A laminated chip element, comprising:

at least one first sheet on which a first conductive pattern is formed, the first conductive pattern consisting of first to third portions, the first and third portions being spaced apart from each other at both ends of the first sheet, the second portion connecting the first and third portions to each other to have a predetermined inductance; and

at least one second sheet on which a second conductive pattern is formed in a transverse direction of both the ends of the first sheet;

wherein the first and third portions are connected to first and second external terminals, respectively, at least one ends of the second conductive pattern is connected to a third external terminal, a plurality of the first sheets and the second sheets are alternately laminated on each other, and the first and third portions of the first conductive patterns formed on the respective first sheets are connected to the respective first and second external terminals.

24. A laminated chip element, comprising:

at least one first sheet on which a first conductive pattern is formed in a direction of both ends of the first sheet; and

at least one second sheet on which a second conductive pattern is formed in the same direction as the first conductive pattern;

wherein both ends of the first conductive pattern are connected to first and second external terminals, respectively, a terminal connecting portion of the second conductive pattern is connected to a third external terminal, and the first and second sheets are laminated.

25. The laminated chip element according to claim 24, wherein the terminal connecting portion is an end of the second conductive pattern.

26. The laminated chip element according to claim 24, wherein the terminal

connecting portion is an intermediate portion of the second conductive pattern.

27. The laminated chip element according to claim 24, wherein the terminal connecting portion is both opposite ends of the second conductive pattern.

28. The laminated chip element according to claim 24, wherein a plurality of the first and second conductive patterns are formed in parallel with each other on the corresponding sheets, the terminal connecting portion of outermost one of the second conductive patterns is connected to the third external terminal, the terminal connecting portions of the other second conductive patterns are connected to the terminal connecting portions of the adjacent second conductive patterns, and both ends of each of the first conductive patterns are connected to the first and second external terminals for each unit element.